ASIC Wafer Test System for the ATLAS Semiconductor Tracker Front-End Chip

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***Abstract*--An ASIC wafer test system has been developed to provide comprehensive production screening of the ATLAS Semiconductor Tracker front-end chip (ABCD3T). The ABCD3T[1] features a 128-channel analog front-end, a digital pipeline, and communication circuitry, clocked at 40 MHz, which is the bunch crossing frequency at the LHC (Large Hadron Collider). The tester measures values and tolerance ranges of all critical IC parameters, including DC parameters, electronic noise, time resolution, clock levels and clock timing. The tester is controlled by an FPGA (ORCA3T) programmed to issue the input commands to the IC and to interpret the output data. This allows the high-speed wafer-level IC testing necessary to meet the production schedule. To characterize signal amplitudes and phase margins, the tester utilizes pin-driver, delay, and DAC chips, which control the amplitudes and delays of signals sent to the IC under test. Output signals from the IC under test go through window comparator chips to measure their levels. A probe card has been designed specifically to reduce pick-up noise that can affect the measurements. The system can operate at frequencies up to 100 MHz to study the speed limits of the digital circuitry before and after radiation damage. Testing requirements and design solutions are presented.**

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I. Introduction

The ATLAS Collaboration, due to start data taking in 2006, is currently entering the production phase for all the detector subsystems. The Semiconductor Tracker (SCT) is one of the key subsystems, featuring an unprecedented tracking volume instrumented with silicon strip modules, with about 6 million channels to read out. The aggressive construction schedule and the large scale of the project amplify the traditionally mild issues in building a detector for a high energy physics experiment. One of them is the necessity to perform comprehensive tests of the front-end chips on a wafer level, in order to use the preselected sample in module construction. A highly specialized system is required.

We have designed and built an ASIC wafer test system to provide production wafer screening of the ATLAS SCT front-end chip (ABCD3T). The features of the ABCD3T are introduced in Section II. The overview of the test system is given in Section III. The tests are described in Section IV.

II. The ABCD3T Chip

Here we give only a short overview of the main features of the chip. More detailed description can be found elsewhere [1]-[4]. The ABCD3T, realized in the radiation hard DMILL

technology, features a 128-channel analog front-end consisting of amplifiers and comparators, and a digital pipeline and communication circuitry. The chip operates at the LHC (Large Hadron Collider, the machine which will be used for the ATLAS experiments) bunch crossing frequency of 40 MHz. Because of the moderate spatial resolution requirements, the IC utilizes a binary readout scheme where the signals from the silicon detector are amplified and then compared to a threshold. Only the result of this comparison, based on a hit or no-hit logic, is stored in the digital pipeline. The chip is capable of latching the data in either edge or level sensing mode and of sparsifying the data according to four different criteria. The binary readout has the advantages of relieving the burdens of the power consumption, cost and the data transmission. For each channel, there is an internal 4-bit DAC to trim the common threshold in order to correct for the channel-to-channel variation and degradation due to the radiation damage. The ABCD3T contains a dedicated charge injection circuitry to calibrate the performance of the analog part by issuing calibration pulses with variable amplitude and delay relative to the clock. Each half of a module in the detector contains six ABCD3T chips, one of which is a "master" communicating with the outside world, and the rest are "slaves", transmitting the data to the neighbor until they reach the "master". Therefore, the digital part of the chip includes the data and token exchange circuitry. Most of the communication signals are duplicated to mitigate the effect of a circuit or a chip failure in the high radiation environment of the LHC.

III. System Overview

A. Components

The ASIC wafer test system, which consists of several custom designed PC boards and control software, has been conceived and built to meet all of the ABCD3T testing requirements. The system architecture is presented in Fig. 1.

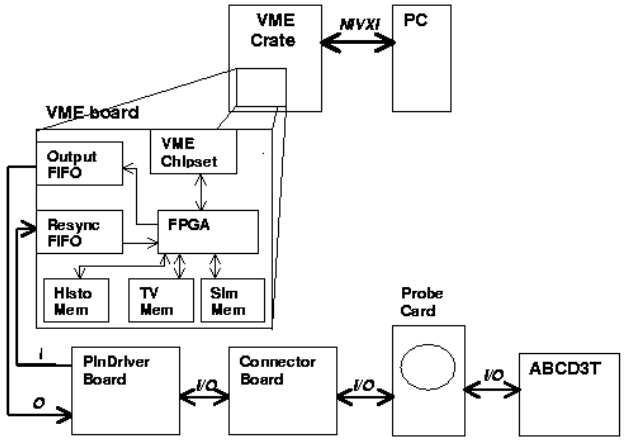

Fig. 1. The architecture of the ASIC wafer test system. All hardware parts of the system and their communication are shown.

The system is controlled by a GUI written in Visual C++, which runs in a PC under Microsoft Windows (W95/NT/2000). The GUI is based on the code for the previous version of the test system [5]. The PC communicates with the VME crate using the NI-VXI interface from National Instruments.

The crate houses a custom-designed VME board equipped with an ORCA3T FPGA of 186000 gates. The FPGA interprets the VME commands, communicates with the ASIC, and controls most critical parameters in the system. The FPGA operates at 40 MHz and is programmed in VHDL.

The data between the VME board and the probe card are transmitted as differential signals. Two intermediate boards have been designed and built to provide:

1) High current pin drivers for inputs with variable signal level

2) Signal delays

3) Window comparators discriminating on the upper and lower output signal levels

4) Dedicated ADCs to probe the internal ABCD3T parameters: power consumption and feedback control of voltages supplied to the chip and ambient temperature of the pin driver board.

For all signals, the pin-driver and window comparator levels and delays are controlled by the FPGA via dedicated DACs.

A probe card has been designed specifically to reduce the pick-up noise that can affect the analog measurements. Digital and analog signals are separated on different planes. An analog ground layer as well as a split digital/analog ground layer are used and low frequency filters are applied to the differential lines that control the analog part of the chip. All the decoupling capacitors are located as close as possible to the probe pins.

B. Design Considerations

To satisfy the schedule for the construction of the ATLAS SCT, wafer screening production rate must exceed two wafers per day per testing site. Therefore the test system must be very fast. The system design was heavily influenced by this requirement.

For the analog tests, the FPGA was programmed to be able to issue a sequence of the ABCD3T input commands, which can be looped over a given number of times. A typical sequence is the calibration pulse command followed by the trigger. The spacing between the commands is controlled by the user. Furthermore, a dedicated datastream-decoding algorithm was conceived to interpret the data from the chip and to extract the numbers of channels having hits. The count of the number of hits for each channel is kept, stored in a memory chip on the VME board. The number of hits per channel, together with the decoding algorithm error codes, is the only information from the test to be read out. This scheme minimizes the amount of information transferred from the VME board to the PC.

The functions of the digital circuitry of the IC are verified using test vectors, which define the sequence of the IC's control line values for consecutive clock cycles. The IC's

output signals are transmitted to the FPGA and compared with the expected data corresponding to that particular test vector. Only the binary result of the comparison is read out. Both the stimulus test vector and the expected chip response are stored in memory chips on the VME board, which makes it possible to run the test vector multiple times without reloading. The expected chip response was obtained with Verilog simulation of the ABCD3T chip design. The FPGA algorithms do not interfere with the test vector content, which allowed for rapid test vector development without firmware changes.

It has been shown that radiation damage slows some digital circuits [4]. To evaluate ABCD3T performance after irradiation, the test vectors are run at frequencies higher than the nominal 40 MHz. This capability is achieved by buffering the signals in FIFOs, which are able to perform the read/write operations at different frequencies. The data exchange between the FPGA and the FIFOs is done at 40 MHz, and the data flow between the FIFOs and the probe card can be done at a different frequency, in the range between 40 and 100 MHz. The higher frequency is obtained using a phase lock loop circuit on the VME board. The frequency is controlled by the FPGA.

The FPGA program followed the rules of modular design, with separate blocks for the analog tests capabilities, test vectors, frequency setup, DACs setup and ADCs readout. As the result, the debugging of the system was greatly simplified, and some simultaneous operations were allowed, such as measuring the power consumption while sending triggers to the chip.

Attention was given to the system reliability issues. There is feedback monitoring of the following crucial quantities:

1) the digital and analog voltages on the ABCD3T

2) the positioning of the probe card relative to the wafer during the test

3) the temperature of the connector board, which is the hottest place in the system, due the presence of the high-current pin driver chips.

The software organization follows staged design with clearly separated functions:

1) The acquisition software compresses the data and stores them in data files. There is no data analysis at this step, the online computer is relinquished from the time-consuming calculating tasks.

2) On the second stage, the data are analyzed using a powerful cluster of Linux computers at CERN. The parameters characterizing a chip are extracted. The chips are classified according their performance. ROOT [6] framework is extensively used at this stage.

3) The chip characteristic parameters are stored in SCT Oracle Database at the University of Geneva for later retrieval by module builders.

Since there is no data analysis done by the online software, it is possible to spend testing time on low quality chips. We have developed two special procedures to speed up the screening in such cases. The first procedure tests the communication with the ABCD3T configuration register. All other tests are skipped if the communication is not successful. The second test scans the digital pipeline of the chip. There is a possibility to skip the remaining tests if the pipeline is not perfect. We currently do not select on the results of this test, but rather reserve this possibility for the scenario of receiving wafers with continuously low yield.

Finally, a statistical study was done to tune the repetition parameters in order to minimize the wafer screening time while maintaining the necessary precision [7].

IV. Testing Procedures

We test the performance of the analog part of the chip, digital part, their power consumption, several internal DACs and the relative phases and levels of the I/O signals.

A. Analog Tests

The basic method for the characterization of the analog circuitry of the ABCD3T consists of an efficiency scan for different threshold values with a fixed calibration charge. A typical “S-curve” from this measurement is shown in Fig. 2, fitted to a complementary error function. The 50% point indicates the threshold value, which corresponds to the injected charge after amplification, and the width characterizes the noise.

To measure the gain and offset, we do the scan at four different calibration input charges. From the 50% points the response curve is plotted and fit to a straight line. The gain is taken as the slope of the fit (Fig. 3, 4).

To characterize the trim DACs, we do the scan of DAC bits for all channels and a fixed calibration pulse. A measure of linearity is obtained in a procedure analogous to the gain extraction.

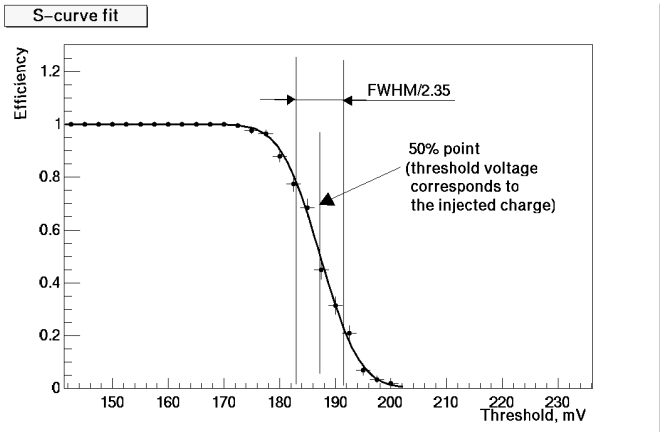

Fig. 2. Example of a threshold scan for a singe channel with fixed injected charge. This is a basic method to study the performance of a binary chip. The midpoint of the transition gives the value of the threshold equal to the injected pulse after amplification. The width of the transition measures the electronic noise. The histogram is fit to a complementary error function.

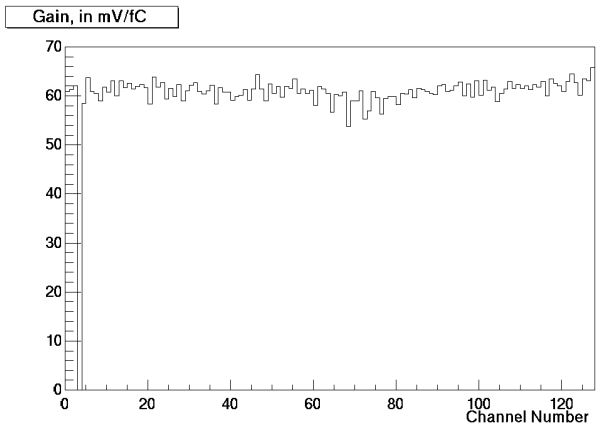

Fig. 3. Gain in mV/fC for the 128 channels on one ABCD3T. Channel number 4 is dead.

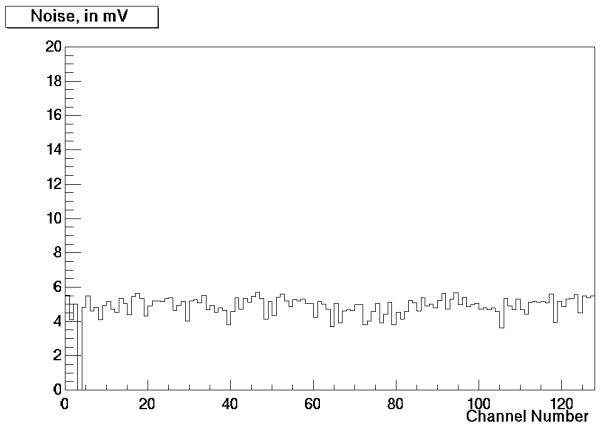

Fig. 4. Noise in mV for the 128 channels on one ABCD3T. Channel number 4 is dead.

B. Digital Tests

The test vectors have been developed to characterize the performance of different parts of the digital circuit. The following set is used in the test:

- Configuration register R/W test.

A value is written to the ABCD3T configuration register, then the chip is set to present the content of the register on the output, and the values are compared. All bits of the ABCD3T configuration register are scanned.

- Addressing, beam counter and the error code test.

The chip possesses an addressing scheme to distinguish different chips on a module. The counter of the LHC beam crossings is embedded in the output data to separate the information from different events. The bits of both counters are scanned. In addition, abnormal conditions are created and the chip response is verified.

- Data compression logic test.

Functionality of four different criteria for data sparsification is verified. Hits are placed in different time slices relative to the trigger.

- Dynamic digital pipeline test.

The digital data are supplied to the input register of the digital circuit according to channel mask. Time structure of the pipeline is scanned.

- Static digital pipeline test.

The digital data are supplied directly to the pipeline, avoiding the input register.

- Redundant command line test.

The dynamic pipeline test is performed using the redundant input command and clock lines.

- Data and token (by)passing circuitry test.

The inter-chip communication functions are tested.

The test vectors are run at a set of frequencies between the nominal 40 MHz and 90 MHz to infer the performance after the irradiation. The scan over the digital voltage within 5% of the nominal 4.0V is also performed. The lower range of the scan is extended to monitor the quality of the probe card contact with the chip pads. The problems with the contact are revealed by non-monotonic dependence of test vector efficiency on the voltage.

C. Power Consumption

We determine the power consumed by the chip by measuring the currents, separately for the digital and analog parts. To simulate the conditions of the experiment, the 100 kHz trigger rate is set while random 3% of channels have hits. The measurement is done separately for the "master" and "slave" modes. Chips with power consumption outside of 30% margin from the wafer mean value are rejected.

D. Internal DACs

The design of the ABCD3T offers capabilities to test its internal DACs by presenting their values on the output pads. The comparator threshold voltage, input transistor bias current and shaper current DACs can be tested. We verify their performance by doing a full scan of the respective DAC bits and measuring the voltage values with the test system ADC. The linearity of the DACs is extracted and compared with specifications.

E. I/O Signals Tests

We test the properties of ABCD3T input or output signal by using test vector stimulating the signal and varying the test conditions.

We test the phases of the input signals, relative to the input clock, by scanning their delays. Test vector efficiency decreases when the corresponding signal is in phase with the clock inside the chip.

We test the phases of the output signals, relative to the input clock, by scanning the delay for the data receiving register latching clock and using the measurements of the signal propagation times in the system.

We vary the swing of the input differential signals to measure the minimal working value.

We vary the thresholds of the window comparators, placed after differential operational amplifiers, to measure the swing of the output differential signals.

Finally, we vary the duty cycles of the input clocks from 40 to 60% to ascertain the stability of the chip performance against the clock shape variation.

The specifications of the I/O properties do not reject a sizable fraction of the chips, however it is important to measure them to monitor fabrication quality, and to select better matching chips when building a module. An example of the distribution of an output signal phase for a wafer is shown in Fig. 5.

V. Yield Calculation

The chips are characterized by their performance in digital tests, matching of the analog characteristics, DAC linearities and power consumption values compared to the specifications and the range of I/O characteristics. Chips meeting the requirements with all channels functional are selected for module construction. We also select a sample of chips with one bad channel, which are otherwise functional, to use for various studies and system development.

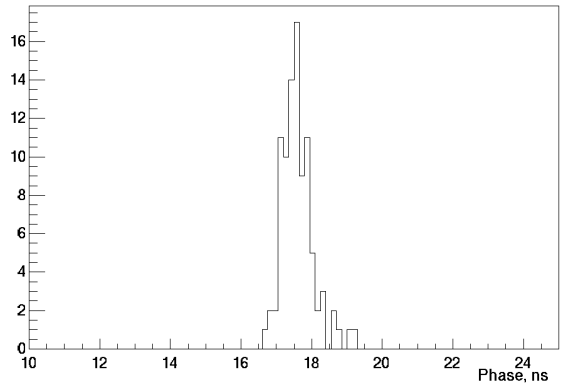

Figure 5 Distribution of the phase of the output data signal for chips with good digital circuitry from one of the wafers. The phase is measured relative to the input clock. The specification range is from 12 to 33 ns.

VI. Concluding Remarks

Test systems have been deployed at the following three ATLAS Semiconductor Tracker institutions: University of California at Santa Cruz, CERN and Rutherford Appleton Laboratory. The performance of the systems has been verified using a common set of reference wafers. The yield was found to agree within 1% for all test sites.

The production of wafers with final version of the ABCD3T chips has started, and the first batch was screened.

The test time was optimized. The time to screen one wafer containing 256 ABCD3T chips is about 5 hours.

VII. Acknowledgment

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VIII. References

[1] ABCD3T ASIC, Project Specification, Version 1.3, http://scipp.ucsc.edu/groups/atlas/prr-doc/ABCD3TA_spec_v1.3.pdf , unpublished.

[2] T. Dubbs et al, "The Development of the CAFE-P/CAFE-M Bipolar Chips for the ATLAS Semiconductor Tracker", Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, CERN/LHC/99-33, p.123.

[3] D. Campbell et al, "The Development of the Rad-Hard CMOS Chip for the Binary Readout of the ATLAS Semiconductor Tracker", Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, CERN/LHC/99-33, p.152.

[4] W. Dabrowski et al, "Radiation Hardness of the ABCD Chip for the Binary Readout of Silicon Strip Detectors in the ATLAS Semiconductor Tracker", Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, CERN/LHC/99-33, p.113.

[5] C. Lacasta and J. Kaplon, "Wafer Screening of the Front-End ASICSs for ATLAS SCT", Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, CERN/LHC/99-33, p.133.

[6] Root: An Object Oriented Data Analysis Framework, http://root.cern.ch/ , unpublished.

[7] C. Flacco, A. Ciocio, and V. Fadeyev, "Optimization of Repetition Parameters for ABCD3T Chip Analog Tests", unpublished.